UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,672	02/27/2002	Jered Donald Aasheim	MS1-1026US	6395

22801 7590 11/08/2005

LEE & HAYES PLLC
421 W RIVERSIDE AVENUE SUITE 500
SPOKANE, WA 99201

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/087,672	Applicant(s) AASHEIM ET AL.	
	Examiner Hetul Patel	Art Unit 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 October 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *03* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-44*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☒ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☒ Other: See Continuation Sheet.

MATTHEW D. ANDERSON
PRIMARY EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: 7. As to the remark, Applicant asserted:
(a) Ban fails to disclose "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1.
(b) Ban also fails to disclose "flash media logic configured to interact with different types of the flash memory media".
(c) Ban fails to disclose "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media". Rather, under Ban the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip only.
(d) Under Ban the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing). Therefore, the CPU, and not the flash driver, provides the flash address at which a read or write operation is to take place. This is opposite of what claimed in claim 9.
(e) Unlike claim 16, where programmable flash medium logic may be programmed by a user to interact with a flash memory medium, under Ban a new controller must be chosen to interact with each new flash chip. Therefore, Ban fails to disclose or show both "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium".
(f) Ban does not disclose "programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected" as recited in claims 23 and 44.
(g) Ban does not disclose "issuing physical sector commands directly to the flash memory medium from a flash medium logic" as recited in claim 33.
(h) Ban fails to disclose the computer readable medium for a flash driver of claims 42-44 because a single controller under Ban cannot provide interface between "one of a plurality of different flash memory media".
(i) Ban does not disclose a flash driver which can "manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic" as recited in claims 43-44.

Examiner respectfully traverses Applicant's remark for the following reasons:
With respect to (a), Ban teaches the flash abstraction logic, i.e. the whole group of interfaces/controllers, between the CPU and the flash memory (e.g. see Fig. 2). Therefore, even though a unique controller is being placed on each individual flash chip, "the group of interfaces/controller" as a whole manages flash memory operations without regard to the type of the one or more flash memory media as being claimed.
With respect to (b), Ban also teaches that the flash media logic, i.e. the group of translation apparatuses/the simple discrete logic in Fig. 1, configured to interact with different types of the flash memory media. Therefore, even though a translation apparatus within a unique controller is configured to interact with an individual flash chip, "the group of translation apparatuses" from all controllers in the array of controllers in Fig. 2 as a whole does interact with different types of the flash memory media as claimed.
With respect to (c), as described above in response to (a) and (b), Ban does teach that the flash abstraction logic (i.e. the whole group of interfaces/controllers, between the CPU and the flash memory in Fig. 2) invokes the flash media logic (i.e. the group of translation apparatuses/the simple discrete logic) to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media (e.g. see the abstract, Col. 2, lines 36-48; Col. 4, lines 33-39, 61-65 and claim 2).
With respect to (d), Examiner like to point out that according to claim 9 of this application, the flash driver is just mapping a logic sector status from the file system to a physical sector status of the flash memory medium, i.e. the claim 9 does not specifically claiming about mapping the logical address to the corresponding physical address. Ban clearly teaches that the logic sector status from the file system (i.e. the standardized commands received from the CPU) is translated/mapped by the flash driver (i.e. the standardized controller translating apparatus) into the physical sector status of the flash memory medium (i.e. commands specific to the type of the flash chip present) (e.g. see Col. 5, lines 29-38).
With respect to (e) and (f), Ban also teaches that the flash media logic (i.e. apparatuses/the simple discrete logic) comprising either a FPGA or an ASIC and the FPGA is the user programmable device, having programmable entry points that can be implemented by a user, as claimed. Furthermore, as disclosed in Col. 2, lines 65+, Ban teaches that the standardized controller is configured to read, write and erase data to and from a flash memory medium.
With respect to (g), Ban does teach about issuing physical sector commands directly to the flash memory medium (array of flash chips) from a flash medium logic (array of flash controllers) (e.g. see Fig. 2).
With respect to (h) and (i), Examiner agreed with the Applicant that a single controller cannot provide an interface between one of a plurality of different flash memory media, however, Examiner would like to point out that the flash driver is (compared with) a group of interfaces/controllers between the CPU and the flash memories taught by Ban. Therefore, the flash driver, i.e. group of interfaces/controllers between the CPU and the flash memories, does provide interface between one of a plurality of different flash memory media and does manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic as claimed. Ban also teaches that a flash driver (a group of interfaces/controllers between the CPU and the flash memories) which provides an interface between a file system (CPU) and a flash memory medium (flash chips) (e.g. see Fig. 2)..

Continuation of 13. Other: The information disclosure statement filed on October 20, 2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because it does not include the certified statements listed under either 37 CFR 1.97(e)(1) or 37 CFR 1.97(e)(2). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 C(1)..